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A Cost-constrained Active Capacitor for a Single-Phase Inverter

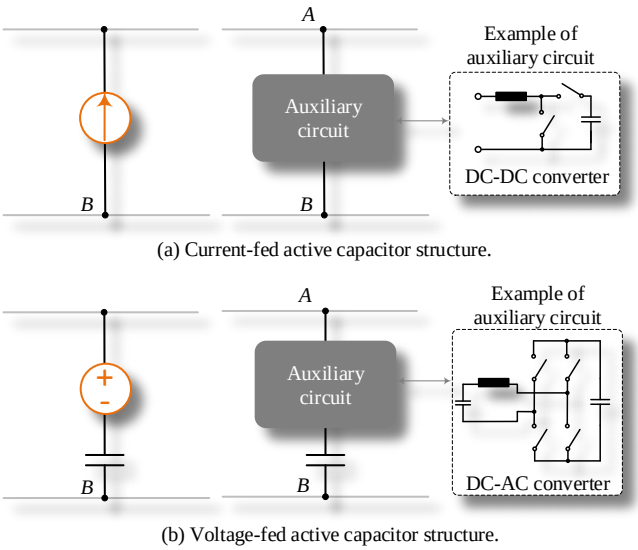
Haoran Wang, *Member, IEEE*, Huai Wang, *Senior Member, IEEE* and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—The active capacitor concept based on power electronic circuits is proposed recently to excess the physical limit of the passive capacitor. It retains the physical convenience of use as a passive capacitor and has the potential to either increase the power density or the lifetime depending on the applications. However, the cost of the existing design by using ceramic or film capacitors to achieve extreme performance increase a lot, which must be taken into account in the design from the industry aspect. This paper proposes a cost-constrained design of an active capacitor used for DC-link applications. It is implemented based on high current electrolytic capacitors instead of film capacitors or ceramic capacitors. A model-based optimization design procedure is discussed in terms of performance factors of interest. A case study of a 5.5 kW single-phase inverter demonstrates a 38% volume reduction of the DC-link with the proposed active capacitor under specific constraints of cost, volume, power loss, and lifetime. The outcomes move one step further for the practical application of active capacitor concept.**

I. Introduction

The most commonly used capacitive DC links are the DC-link capacitors, such as electrolytic capacitors, film capacitors, and ceramic capacitors [1]. Since the performance of the passive capacitors are dependent on the conducting materials and the insulation layer of dielectric materials, with more stringent constraints brought by automotive, aerospace, and energy industries, the design of DC links encounters challenges in terms of power density, weight, reliability, and cost [1, 2].

Instead of using the conventional structure with two plates and dielectric materials, power electronics switching circuits based two-terminal active capacitors are proposed to exceed the physical limitations of the passive DC-link capacitors [3–7]. By taking advantage of the latest Si and Wide Bandgap semiconductor devices and power electronic based solid-state circuits, it is possible to achieve more than two times better performance in lifetime and power density, which otherwise can not be achieved by conventional methods [8–11]. Typically, there are two topologies to implement for the two-terminal active capacitors as shown in Fig. 1, which are current-fed topology implemented by DC-DC power converters [12–15] and voltage-fed topology implemented by a DC-AC power converter with a series buffer capacitor [8, 9]. With the internal signals based control methods, both topologies



(a) Current-fed active capacitor structure.

(b) Voltage-fed active capacitor structure.

Fig. 1. Typical structures of active capacitors. (a) Current-fed active capacitor structure and (b) Voltage-fed active capacitor structure.

having smaller energy storage elements can perform large equivalent capacitance seen from the terminals. The difference is that the auxiliary circuit of the voltage-fed topology handles lower voltage and current stresses as well as less apparent power compared with that in the current-fed topology, and therefore it can achieve higher efficiency, higher power density, and less cost for a specified lifetime in theory. The functionality of the voltage-fed active capacitor has been demonstrated in the DC link of various applications [4, 9]. Depending on the types of buffer capacitors C_1 used in the voltage-fed topologies, existing demonstrations can be divided into two types. The ceramic capacitor stack based voltage-fed active capacitor is proposed for high efficiency and power density in the Google Little Box competition [9–11, 16], and the film capacitor based active capacitor is built for highly reliable PV inverter in a proof of concept [4, 8]. However, from the real industry point of view, the ceramic capacitor and film capacitor versions are hardly to be used practically, due to:

1) Cost is a key factor which needs to be considered in the design phase, where the film and ceramic capacitors are expensive;

2) Film capacitors available on the market are bulky due to the relative low energy density;

3) Energy storage requirement, besides the capacitance demand, are rarely considered, nevertheless, it is relevant to many applications.

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The existing proof-of-concept design can achieve higher power density or longer lifetime, however, the cost is always much higher than the conventional capacitor bank. As part of continuing efforts to overcome the above challenges, this study focuses on addressing the cost issue of active capacitors under additional constraints of lifetime, power loss, and volume. In the existing voltage-fed active capacitor, film or ceramic capacitors are used for the buffer capacitor C_1, which contributes to most volume and cost. From comparison among the three typical capacitors in [1], it can be seen that electrolytic capacitor can also be a capacitor candidate used for C_1. It is able to achieve the lowest cost and volume, but its reliability need to have special concerns during the component sizing procedure, as the electrolyte evaporation under the thermal stress will affect the chemical reactions inside [17–19]. At this time, some specific issues for the electrolytic capacitor based active capacitor should be considered, such as: 1) Ripple current limitation of the electrolytic capacitor; 2) Electrical, power loss, thermal, and lifetime modeling to evaluate the reliability performance; 3) Optimized design to minimize the cost and volume, and the other physical configurations. Indeed, electrolytic capacitors meet challenges from the reliability aspect, but it relies on the applications and component sizing. By reducing the thermal stress as well as the power loss of the capacitor, or using the highly rated lifetime and high current electrolytic capacitors, it is possible to achieve the lifetime target, while the cost and volume are reduced.

In this study, a complete design procedure is proposed for a DC-link active capacitor, which considers the multiple design constraints of commercial products, especially the cost constraint. It has the following features:

1) A design-oriented multi-objective design flowchart with detailed component and circuit modeling is proposed. On the premise of functionality, the encountered trade-offs and parameter inter-dependence are highlighted and analyzed. The solutions, which can achieve the lifetime, cost, volume, and efficiency constraints are identified;

2) The high current electrolytic capacitors, which are always excluded from the database due to the reliability challenge, are for the first time incorporated as the candidates for the buffer capacitors in voltage-fed topology to compete with the film and ceramic capacitors. With a specified mission profile and reliability design, it has the potential to fulfill the lifetime target with less volume and cost;

3) A voltage-fed DC-link active capacitor for a 5.5 kW single-phase inverter is demonstrated to verify the accuracy of the proposed design with multiple design constraints, especially in respect to cost and volume.

The proposed design method with multiple constraints is a general one, which can help the designers to build the commercial DC-link active capacitor with multiple real design constraints in a step by step manner. The rest of this paper is organized as follows. In Section II, the implementation of the passive and active capacitors are discussed and benchmarked; The multi-objective design method considering lifetime, cost, volume, and efficiency will be proposed in Section III. Based on the optimized results, a hardware prototype with the experimental results to verify the accuracy of the multi-objective design solution are presented in Section IV, and then followed by the conclusions.

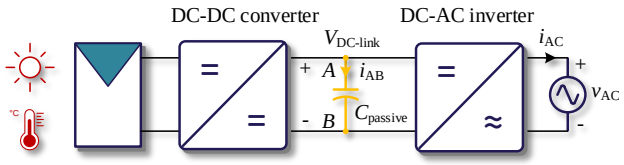

Fig. 2. System structure of a single-phase PV inverter with passive DC-link capacitor.

TABLE I
SPECIFICATION OF A 5.5 KW SINGLE-PHASE INVERTER.

Item	Value	Unit
Power rating	5.5	kW
Grid voltage peak value (V_{m})	220	V
Grid frequency (ω)	314	rad/s
DC-link voltage average value ($V_{\text{DC-link}}$)	320	V
Maximum allowed voltage ripple V_{pp}	10	V
Maximum allowed current ripple ratio of inductor $\alpha_{\text{i}_{\text{L}_\text{f}}}$	20 %	

II. OVERVIEW OF THE SINGLE-PHASE PV INVERTER WITH CAPACITIVE DC LINKS

This section discusses the possible implementations of the capacitive DC link for a 5.5 kW single-phase inverter. The conventional passive DC-link capacitor solution is analyzed first, in terms of lifetime, cost, and volume. Aiming to shrink the volume and keep the similar cost and lifetime level, the active capacitors based on the current-fed and voltage-fed topologies are studied and benchmarked.

A. Single-phase PV Inverter with Typical DC-link Capacitor Bank

Fig. 2 shows the system structure of a 5.5 kW single-phase PV inverter system. The specifications are shown in Table I. DC-DC converter serves as the first stage for Maximum Power Point Tracking (MPPT) and DC-AC single-phase inverter feeds the power into a commercial electrical grid or a local, off-grid electrical network [20, 21]. Due to the capacitive DC link aims to limit the DC-link voltage ripple into V_{pp}, the minimum capacitance used for passive capacitive DC link can be obtained from the following equation [8]

$$C_{\text{passive}} = \frac{\sqrt{2} I_{\text{AB}}}{2\omega \frac{V_{\text{pp}}}{2}} = \frac{V_{\text{m}} I_{\text{m}}}{\omega V_{\text{DC-link}} V_{\text{pp}}} \tag{1}$$

where I_{AB} is the Root Mean Square (RMS) current of the capacitive DC link, V_{pp} is the maximum allowed peak-to-peak DC-link voltage, V_{m} and I_{m} are the amplitude of AC voltage and current, $V_{\text{DC-link}}$ is the average DC-link voltage, and ω is the grid frequency. Based on the specifications shown in Table I, the implementation of the capacitor bank can be obtained as 5640 μF (470 μF/ 450 V*12) electrolytic capacitors, where cost, volume, and lifetime are estimated as 60 USD, 0.8 L, and more than 15 years (8 operating hours per day), respectively [22]. With the development trend for the high power density, the passive capacitor bank becomes the bottleneck of the whole

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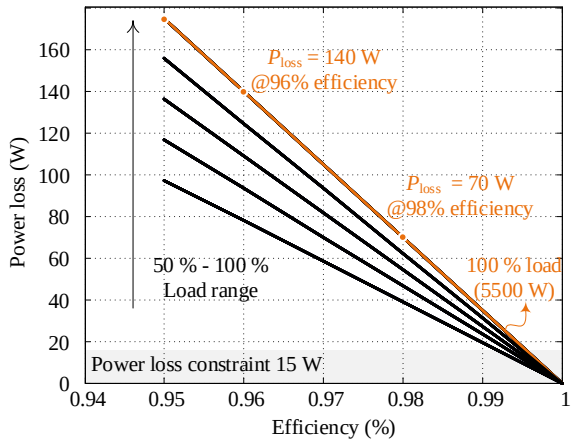

Fig. 3. Relation between the efficiency of the auxiliary circuit and the power loss of the current-fed active capacitor.

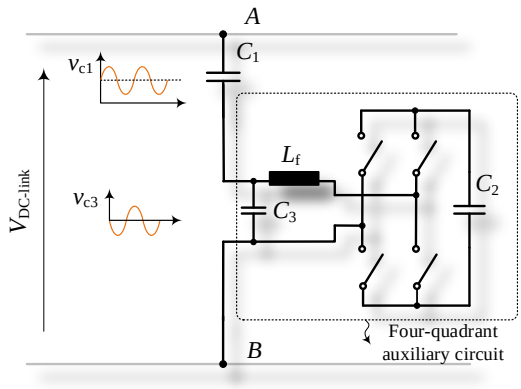

Fig. 4. Voltage-fed active capacitor topology studied in this paper.

system, meanwhile, a new capacitive DC link with smaller size and similar lifetime and cost is expected. Along with this trend, the new design constraints are pointed out and shown in Table II, where the volume reduces to lower than 70 % of the conventional capacitor bank and cost, lifetime, and power loss are kept to the same level.

B. Preliminary Study of Active Capacitor Candidates

The candidates of active capacitor topology are the current-fed and voltage-fed topologies. The distinction of these two solutions is the way of auxiliary circuit connected to the DC link.

1) Current-fed Active Capacitor Topology: Fig. 1(a) presents the topology of the current-fed active capacitor. Due to the auxiliary circuit is connected directly to the DC link, it handles all the DC-link voltage $V_{\mathrm{DC-link}}$ and RMS ripple current I_{AB}. The apparent power processed by the auxiliary circuit is

$$S_{\mathrm{aux}} = V_{\mathrm{DC-link}} I_{\mathrm{AB}} \tag{2}$$

The power loss of the auxiliary is determined by the apparent power handled and the efficiency of itself, which is different from case to case. Based on the specifications shown in Table I, the relationship between the efficiency of the auxiliary circuit and its power loss can be seen in Fig. 3. The power loss is much higher than the 15 W constraint shown in Table II, with the efficiency range from 94 % to 98 %. It means the current-fed topology is hardly to achieve the power loss constraint.

TABLE II
DESIGN CONSTRAINTS OF THE DC-LINK ACTIVE CAPACITOR FOR A 5.5 KW SINGLE-PHASE INVERTER.

Item	Value	Unit
Lifetime	$>$ 15	years
Cost	$<$ 60	USD
Volume	$<$ 0.5	L
Power loss	$<$ 15	W

2) Voltage-fed Active Capacitor Topology: Another capacitive DC-link candidate is the voltage-fed active capacitor topology as shown in Fig. 4. A full-bridge converter is connected in series with a capacitor C_1. It handles only the ripple voltage and ripple current of C_1, implying a low *VA* rating. Thus, it is possible to achieve lower cost, lower power loss, and higher power density compared with the current-fed topology. There is a trade-off between the lifetime, cost, volume, and power loss. Detailed discussions regarding the design optimization will be presented in the next section.

III. Multi-objective Design Considering Lifetime, Cost, Volume and Efficiency

Based on the comparable study in above section, the voltage-fed active capacitor is selected for a 5.5 kW single-phase inverter to fulfill the requirements listed in Table II. In this section, a multi-objective design procedure for the voltage-fed topology is discussed step by step, in terms of design input, design space, performance space, and design results. The analytical equations derived are generic ones and the presented numerical results in the figures are based on a specific design case with the specifications shown in Table I.

A. Design Input

(a) System Specification

The specification of the active capacitor includes the operating conditions and mission profile. The operating conditions such as the power rating and the DC-link voltage determine the maximum stress of individual components, while the mission profile such as the long-term loading conditions and ambient temperature of the inverter system determine the thermal stress of the active capacitor. These aspects affect the component sizing in the design procedure as well as the performance mapping.

(b) Design Constraints

The design constraints, including lifetime, volume, cost, and efficiency, are depending on the applications. Based on the analysis for a 5.5 kW single-phase PV applications in Section II, the design targets for the optimization can be obtained in terms of smaller size and similar cost. In the design procedure, the lifetime is the first constraint need to be achieved besides the functionality. Then, the performance boundaries and design results to fulfill the other constraints can be obtained.

(c) Design Variables

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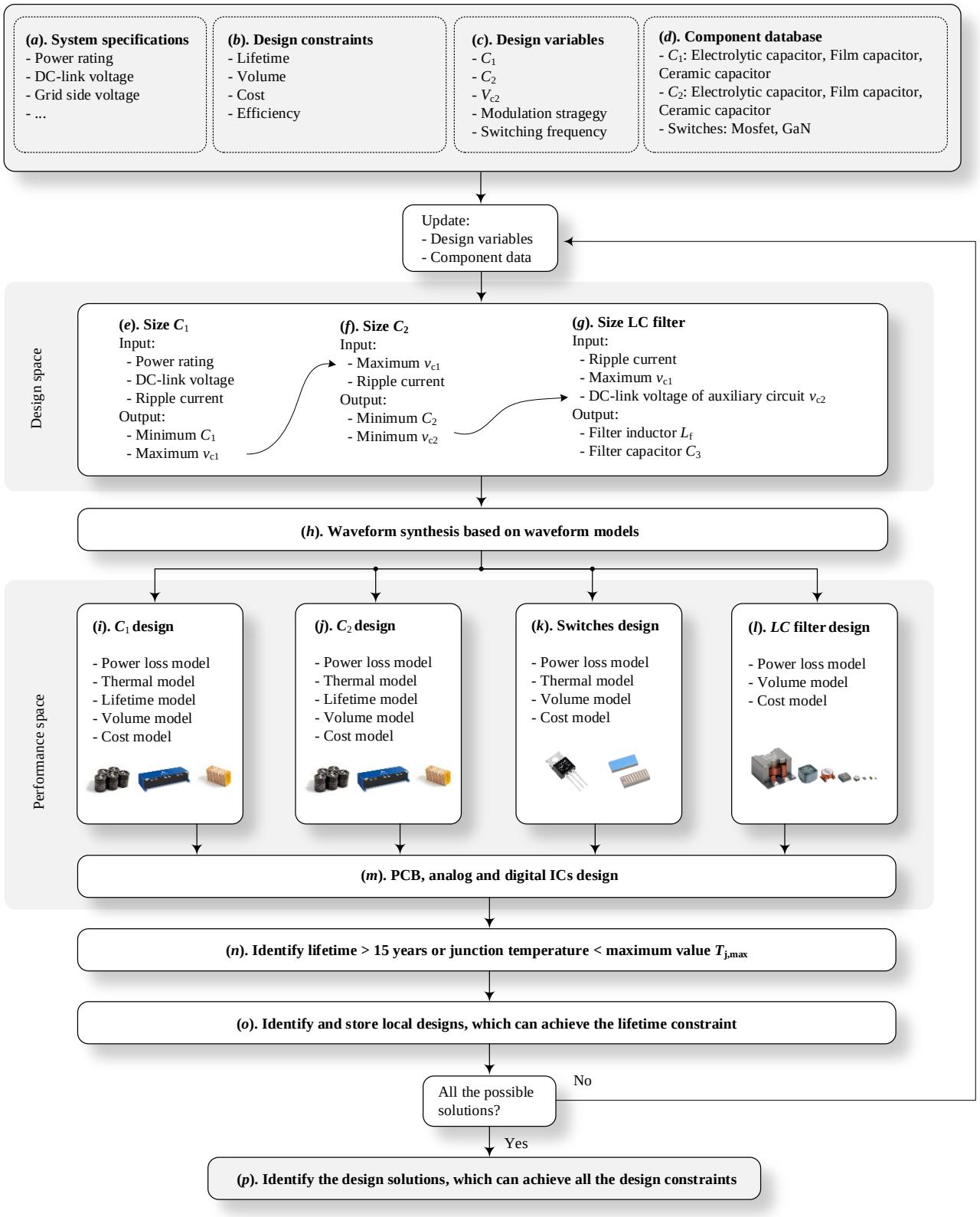

Fig. 5. Flowchart of the life-cycle multi-objective design procedure for the active capacitor.

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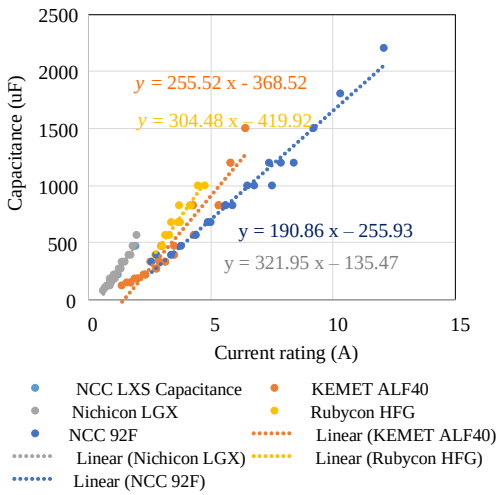
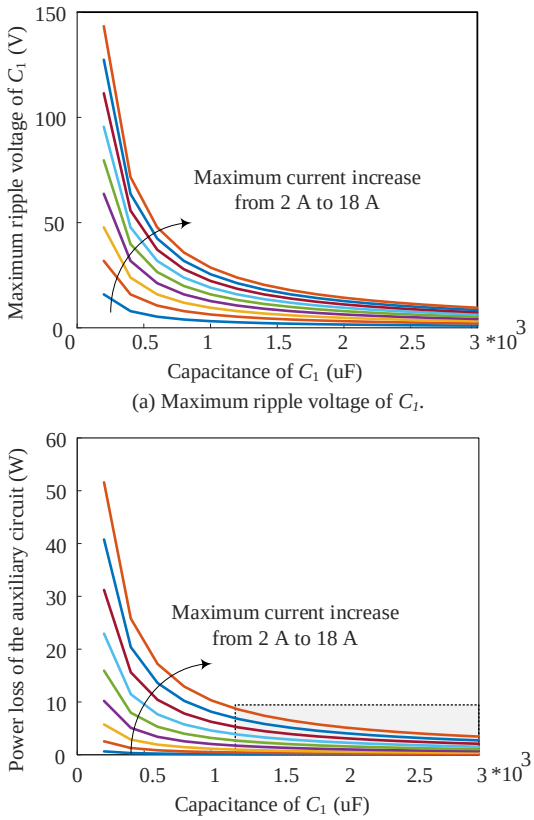


Fig. 6. Capacitor C_1 sizing criteria based on current rating.



(a) Maximum ripple voltage of C_1.

(b) Power loss of the auxiliary circuit when the efficiency assumes to be 98 %.

Fig. 7. Capacitor C_1 sizing criteria based on power loss limitation.

Design variables in the multi-objective optimization can be divided into two groups. The first group is about the components' parameters of the active capacitor, including C_1, C_2 and V_{C_2}. By changing these capacitances and DC-link voltage of the auxiliary circuit, the component waveforms as well as the performance space of the buffer capacitor C_1,

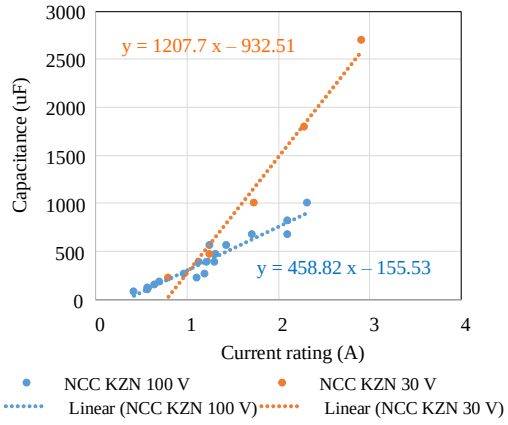


Fig. 8. Capacitor C_2 sizing criteria based on current rating.

DC capacitor C_2, switches, and AC filters will be updated, accordingly. The other group is in respect to modulation in terms of modulation strategies and switching frequency, which affect the electro-thermal stress as well as the performance space of the switches and AC filters. Considering the ranges of design variables, the numbers of design results, which can achieve the design constraints, can be found.

(d) Component Database

Component database has significant impact on the performance of the active capacitor. Electrolytic, film and ceramic capacitors are the candidates for C_1 and C_2 depending on applications. For the same voltage and energy storage level, electrolytic capacitors are cheaper and smaller than film and ceramic capacitors in general. However, the reliability of the electrolytic capacitor is a challenge, so that the lifetime prediction need to be considered seriously in the design phase. For the cost-constrained application in this study, different electrolytic capacitor series in terms of rated lifetime, current capability and power density are taken into account. By sizing and evaluating C_1 and C_2 with different series capacitors, the solutions, which can achieve all the performance constraints, can be selected. In terms of the switches, MOSFET and GaN with different voltage and current capabilities are included in the database.

B. Design Space for the Active Capacitor

(e) Sizing Criteria of C_1

C_1 is the key component to buffer the ripple power, which contributes to high percent of volume, weight, and cost. Ideally, the deeper allowed discharge, the smaller capacitance can be used. However, it can not be as small as possible, due to the limitation of the voltage and current rating of capacitors. When the voltage rating is fully used, the boundary of C_1 can be derived as

$$C_1 \geq \frac{I_{\mathrm{max,ripple}}}{\omega_{\mathrm{ripple}} V_{\mathrm{rating,C_1}}} \tag{3}$$

where $I_{\mathrm{max,ripple}}$ is the maximum current flowing through the active capacitor, ω_{ripple} is the angular frequency of the ripple current, and $V_{\mathrm{rating,C_1}}$ is the maximum voltage allowed,

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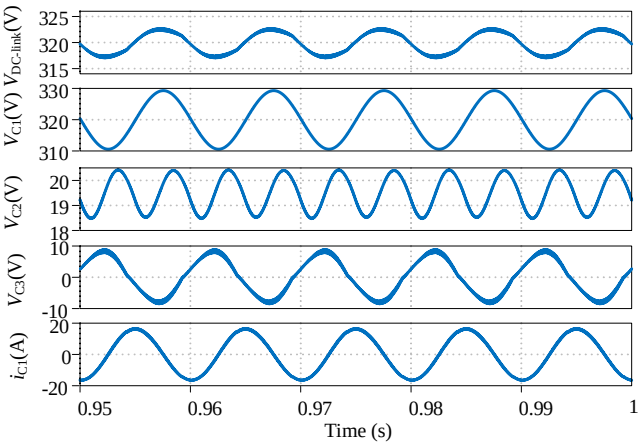

Fig. 9. Simulation waveforms of the key components in an active capacitor.

which is determined by the voltage rating of capacitors with a specified design margin (e.g, 1.5 or 2 times margin).

The current rating of typical electrolytic, film and ceramic capacitors are proportional to the capacitance on the same voltage level. For the film and ceramic capacitors, the current capability are much better than electrolytic capacitors in general [1]. Based on the data from Digikey, the current rating of electrolytic capacitors are statistically and shown in Fig. 6 [22, 23]. The capacitance of the electrolytic capacitor is linear with the current rating. The sizing criteria of C_1 from the current rating perspective can be obtained as

$$C_1 \geq k_{1,\mathrm{C_1-I_{rating}}} I_{\mathrm{rating,C_1}} + k_{2,\mathrm{C_1-I_{rating}}} \tag{4}$$

where $I_{\mathrm{rating,C_1}}$ is the current rating of C_1, which is determined by the maximum ripple current $I_{\mathrm{max,ripple}}$ and design margin. $k_{1,\mathrm{C_1-I_{rating}}}$ and $k_{2,\mathrm{C_1-I_{rating}}}$ are the coefficients from curve fitting.

Power loss of the active capacitor constrains the component sizing of C_1, which depends on the implementation. It includes two parts: the power loss contributed by C_1 and by the auxiliary circuit. With different capacitance of C_1, the maximum ripple voltage of C_1 as well as the voltage stress of the auxiliary circuit will be different, which will affect the power loss of the DC-link active capacitor. Assuming the efficiency of the auxiliary full-bridge circuit can be 98 % and the power loss of the auxiliary circuit is lower than 10 W, the boundary of the C_1 can be obtained as shown in Fig. 7. From above analytical analysis, the range of C_1 with corresponding $v_{\mathrm{C_1}}$ and $v_{\mathrm{C_2}}$ can be obtained, which are the input of the C_2 sizing.

(f) Sizing Criteria of C_2

The sizing criteria of C_2 for stability has been discussed in [24]. To ensure the full-bridge auxiliary circuit operation within the modulation index lower than one, the average DC voltage and the capacitance of C_2 should satisfy the following equation

$$\frac{\sqrt{2}I_{\mathrm{AB}}}{\omega} \leq C_1 V_{\mathrm{C_2,DC}} \sqrt{\frac{2C_2}{2C_2 + C_1}} \tag{5}$$

Due to C_2 is a low-voltage component, the best choice is the electrolytic capacitor from the cost point of view. The sizing criteria from the current rating of electrolytic capacitor C_2 can be found as

$$C_2 \geq k_{1,\mathrm{C_2-I_{rating}}} I_{\mathrm{rating,C_2}} + k_{2,\mathrm{C_2-I_{rating}}} \tag{6}$$

where $I_{\mathrm{rating,C_2}}$ is the current rating of C_2, which is determined by the maximum ripple current $I_{\mathrm{max,ripple}}$ and design margin. $k_{1,\mathrm{C_2-I_{rating}}}$ and $k_{2,\mathrm{C_2-I_{rating}}}$ are the coefficients from the curve fitting.

(g) Sizing Criteria of LC Filter

The inductance of L_{f} is determined by the current ripple ratio. When $v_{\mathrm{C_2}}$ is at its peak and the output voltage of the auxiliary circuit is at zero volt, the maximum inductor current ripple occurs and it can be expressed as [16]

$$\Delta I_{\mathrm{L,max}} = \frac{\sqrt{V_{\mathrm{C_2,DC}}^2 + \frac{(\sqrt{2}I_{\mathrm{AB}})^2}{2\omega^2 C_1 C_2}}}{2L_{\mathrm{f}} f_{\mathrm{sw}}} \tag{7}$$

where f_{sw} is the switching frequency of the auxiliary circuit. The ripple current of the inductor should be limited into the maximum allowed ratio $\alpha_{\mathrm{i_{L_f}}}$ defined in specification as shown in Table I. The sizing criteria of filter capacitor C_3 depends on the requirement of the system. The cut-off frequency of the LC filter should be designed seriously considering the attenuation at specified frequency if there is THD constraint. In this case study, in order to reduce the complexity of the multi-objective design, C_3 is designed according to the cut-off frequency with lower than 1/6 of the switching frequency

$$C_3 \geq \frac{1}{4\pi^2 f_{\mathrm{cut-off}}^2 L_{\mathrm{f}}} \tag{8}$$

(h) Waveform Synthesis

Based on the component sizing, the current and voltage waveforms of individual component can be determined, which are used to map the design space into the performance space. The waveform synthesis is conducted in the time and frequency domain. The waveforms are synthesized for all nominal and worst-case operating points and represent a fundamental prerequisite for the component design. One waveform synthesis example based on the specification in Table I is shown in Fig. 9.

C. Mapping of Design Space Into Performance Space

(i) Performance Space of C_1

Power loss of C_1 is estimated from Equivalent Series Resistance (ESR) and ripple current flowing through the capacitor, which can be expressed as

$$P_{\mathrm{loss,C1}} = \sum_{i=1}^{n} [ESR_{\mathrm{C_1}}(C_1, f_{\mathrm{i}}, T_{\mathrm{h,C_1}}) \times I_{\mathrm{rms}}^2(f_{\mathrm{i}})] \tag{9}$$

where

$$ESR_{\mathrm{C_1}}(C_1, f_{\mathrm{i}}, T_{\mathrm{h,C_1}}) = ESR_{\mathrm{C_1,rated}}(C_1) \times \alpha_{\mathrm{ESR_{C_1}}}(f_{\mathrm{i}}, T_{\mathrm{h,C_1}}) \tag{10}$$

$ESR_{\mathrm{C_1,rated}}(C_1)$ is the ESR at 100 Hz, which is a function of capacitance. Dissipation factor $\tan\delta$ of each kind of product

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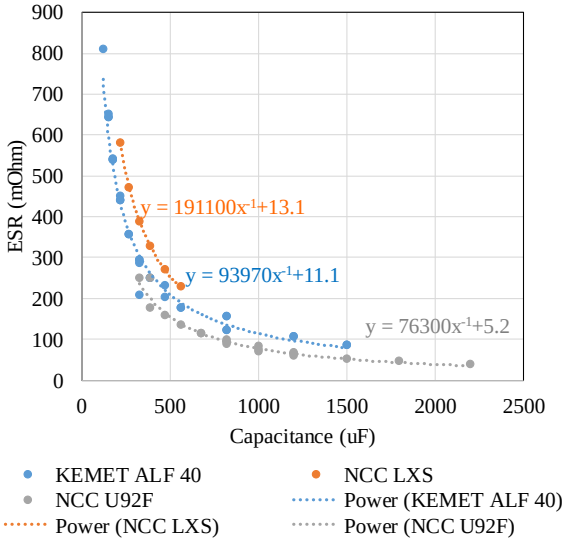

Fig. 10. Relation between capacitance and ESR of C_1.

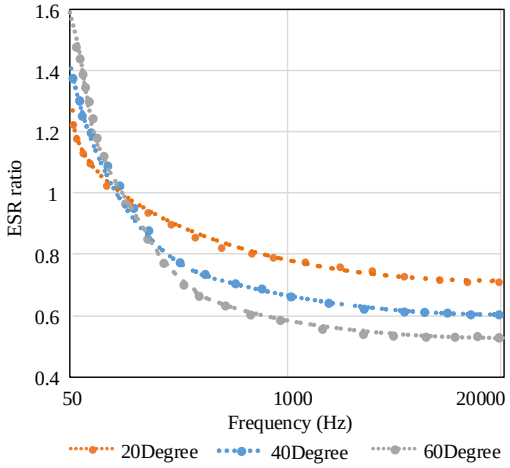

Fig. 11. An example of relation between frequency f_{i}, temperature $T_{\mathrm{h,C_1}}$ and ESR ratio $\alpha_{\mathrm{ESR_{C_1}}}(f_{\mathrm{i}}, T_{\mathrm{h,C_1}})$.

has a constant value, which is defined as the ratio of the ESR and capacitive reactance [25], as shown below

$$\tan\delta = \omega C ESR \tag{11}$$

It can be seen that capacitance and ESR are reciprocal relationships. Therefore, the mathematical model between capacitance and $ESR_{\mathrm{C_1,rated}}$ at 100 Hz is written as

$$ESR_{\mathrm{C_1,rated}}(C_1) = k_{1,\mathrm{ESR_{C1}}} C_1^{-1} + k_{2,\mathrm{ESR_{C1}}} \tag{12}$$

$k_{1,\mathrm{ESR_{C1}}}$ and $k_{2,\mathrm{ESR_{C1}}}$ represent the dielectric material and packaging related coefficients, respectively, which can be obtained by curve fitting as shown in Fig. 10. Due to ESR is temperature and frequency dependent, the ESR ratio for a specified frequency and temperature $\alpha_{\mathrm{ESR_{C_1}}}(f_{\mathrm{i}}, T_{\mathrm{h,C_1}})$ is introduced as shown in (10). By measuring the ESR at a range of frequencies and temperatures, $\alpha_{\mathrm{ESR_{C_1}}}(f_{\mathrm{i}}, T_{\mathrm{h,C_1}})$ can be obtained, which is shown in Fig. 11. The testing equipments to obtain the ESR is shown in Fig. 12.

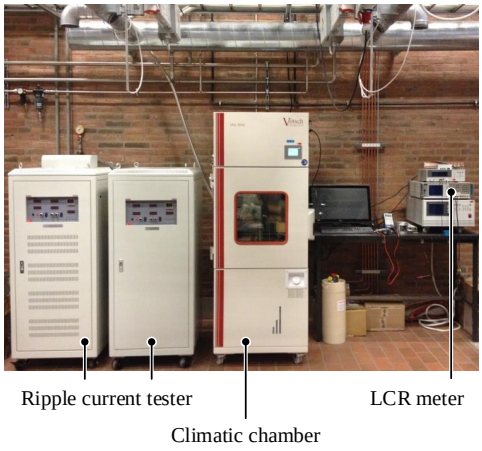

Fig. 12. Testing setup at Aalborg University for characterizing different capacitors.

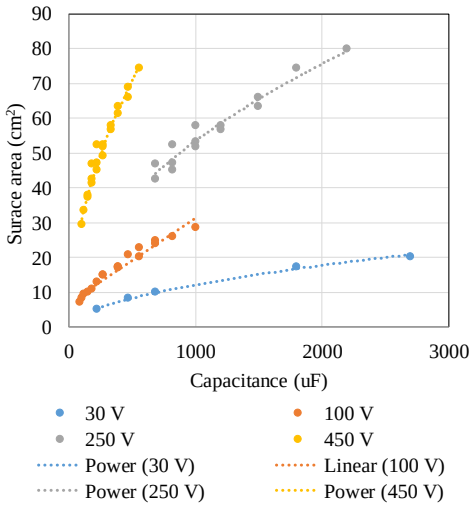

Fig. 13. Relation between capacitance, voltage and surface area of electrolytic capacitors.

Thermal stress is one of the critical stressors of capacitors, resulting in the reduction of capacitance and the increase of ESR due to wear out [26]. In electrolytic capacitors, the dominant degradation mechanisms are electro-chemical reaction in the oxide layer and the electrolyte vaporization [19]. The current ripple and ambient temperature are the contributors to the internal thermal stress of capacitor. Especially, the increase of capacitor power loss causes a higher operating temperature inside of capacitor. The hot-spot temperature of capacitor, which is affected by the power loss and ambient temperature, is derived as

$$T_{\mathrm{h}} = T_{\mathrm{a}} + R_{\mathrm{ha}} \times P_{\mathrm{loss,C1}} \tag{13}$$

where T_{h} is the hot-spot temperature, T_{a} is the ambient temperature and R_{ha} is the equivalent thermal resistance from hot-spot to ambient. The hot-spot temperature T_{h} can then be estimated. Thermal resistance of the capacitor ignores the heat dissipation from the pins and PCB. Therefore, only heat convection and radiation transfer from surface are considered for the capacitor. Thermal resistance from hot-spot to ambient

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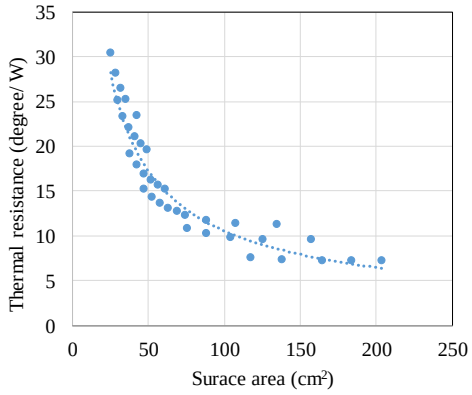

Fig. 14. Relation between surface area and thermal resistance of electrolytic capacitor.

is an inverse proportional function of surface area of the capacitor [25]. Therefore, it can be written as

$$R_{\mathrm{th}} = k_{1,\mathrm{R_{th}}} A^{-1} + k_{2,\mathrm{R_{th}}} \tag{14}$$

where $k_{1,\mathrm{R_{th}}}$ and $k_{2,\mathrm{R_{th}}}$ are the coefficients of thermal resistance model. The surface area is determined by the energy storage, electric charge, voltage rating, and capacitance

$$A = k_{1,\mathrm{A}} CV^2 + k_{2,\mathrm{A}} CV + k_{3,\mathrm{A}} V + k_{4,\mathrm{A}} \tag{15}$$

$k_{1,\mathrm{A}}$, $k_{2,\mathrm{A}}$, $k_{3,\mathrm{A}}$ and $k_{4,\mathrm{A}}$ are the coefficients of the surface area model.

Lifetime prediction for capacitors can be done by the model which predicts the lifetime of capacitors under different operation conditions [27]. For electrolytic capacitor and film capacitors, a simplified model from the above equation is popularly applied given as:

$$L = L_0 \times (\frac{V}{V_0})^{-n} \times 2^{\frac{T_0 - T}{10}} \tag{16}$$

The model corresponds to a specific case of first equation when $E_{\mathrm{a}} = 0.94eV$ and T_0 and T are substituted by $398K$. For electrolytic capacitors, the value of *n* typically varies from 3 to 5.

Volume and cost of electrolytic capacitor are linear with the energy storage, which is $E_{\mathrm{cap}} = \frac{1}{2}CV^2$. Therefore, they are linear with the capacitance for the same voltage rating. The volume and cost models of several electrolytic capacitor series are shown in Fig. 15 and Fig. 16, respectively, and the mathematical model are given as

$$Volume_{\mathrm{C_1}} = k_{1,\mathrm{C_1-vol}} C_1 + k_{2,\mathrm{C_1-vol}} \tag{17}$$

$$Cost_{\mathrm{C_1}} = k_{1,\mathrm{C_1-cost}} C_1 + k_{2,\mathrm{C_1-cost}} \tag{18}$$

where the coefficients of $k_{1,\mathrm{C_1-vol}}$ and $k_{1,\mathrm{C_1-cost}}$ represent the energy storage related volume and cost, and $k_{2,\mathrm{C_1-vol}}$ and $k_{2,\mathrm{C_1-cost}}$ represent the package volume and cost, respectively. All the coefficients can be extracted from curve fitting.

(j) Performance Space of C_2

C_2 is a low-voltage component, where a low-voltage electrolytic capacitor is used. The performance spaces of C_2 are similar with that of C_1, while the coefficients for each model

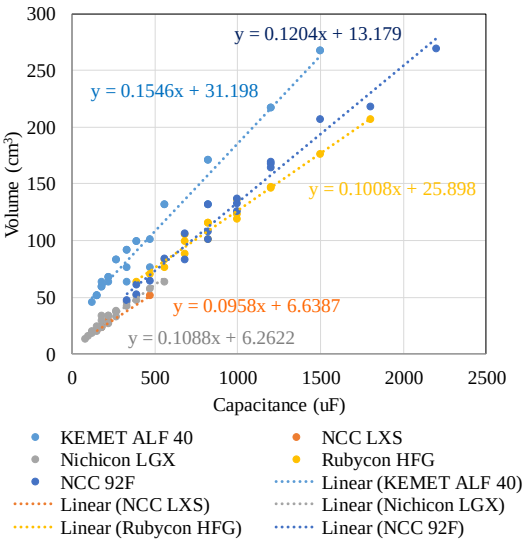

Fig. 15. Relation between capacitance and volume of electrolytic capacitor C_1.

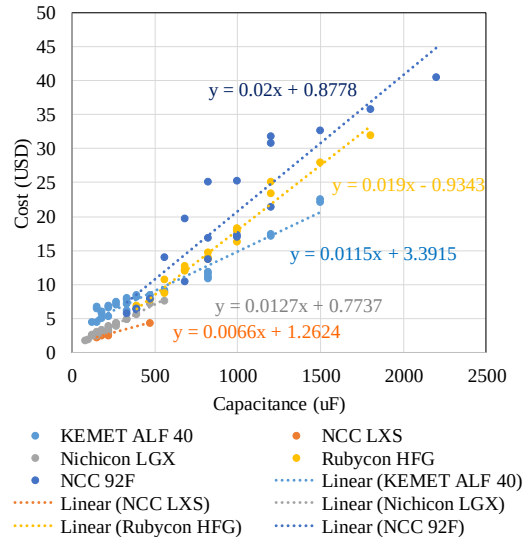

Fig. 16. Relation between capacitance and cost of electrolytic capacitor C_1.

need to be updated. The ESR, volume and cost models of C_2 are shown in Fig. 17, Fig. 18 and Fig. 19, respectively.

(k) Performance Space of Switches

The power losses of power semiconductor devices consist of the conduction loss and switching loss. If it is assumed that the current and voltage in a switching period is constant, the conduction loss in a switching period of each power device is

$$P_{\mathrm{con_T}} = R_{\mathrm{ds,on}}(|i_{\mathrm{sw}}|, T_{\mathrm{j}}) i_{\mathrm{sw}}^2 \tag{19}$$

where $P_{\mathrm{con_T}}$ is the conduction loss of the active device, i_{sw} is the current flowing through the device, and T_{j} is the junction temperature of the device. $R_{\mathrm{ds,on}}$ is the on-state resistance. On the other hand, the switching loss in each power device can be calculated as

$$P_{\mathrm{sw_T}} = f_{\mathrm{sw}}[E_{\mathrm{on}}(|i_{\mathrm{sw}}|, T_{\mathrm{j}}, V_{\mathrm{dc}}) + E_{\mathrm{off}}(|i_{\mathrm{sw}}|, T_{\mathrm{j}}, V_{\mathrm{dc}})] \tag{20}$$

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TABLE III
LIFE-CYCLE MULTI-OBJECTIVE OPTIMIZATION RESULTS

	C_1	C_2	L_f	Switches	Others	Total	Prototype
Cost (USD)	26.1	2.34	2.65	12	10	54	58
Volume (L)	0.3	0.02	0.009	0	0.1	0.454	0.49
Power loss (W)	5.4	0.83	0.87	3.5	5	15.6	14.3

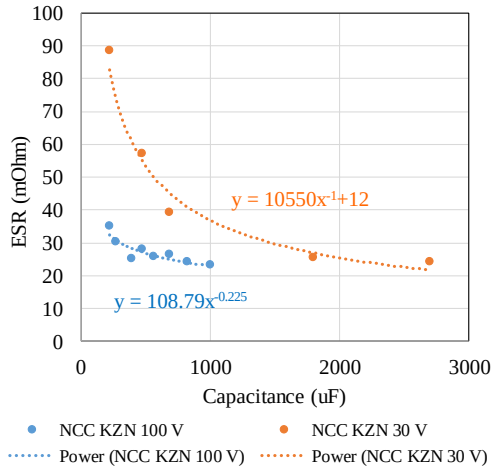

Fig. 17. Relation between capacitance and ESR of electrolytic capacitor C_2.

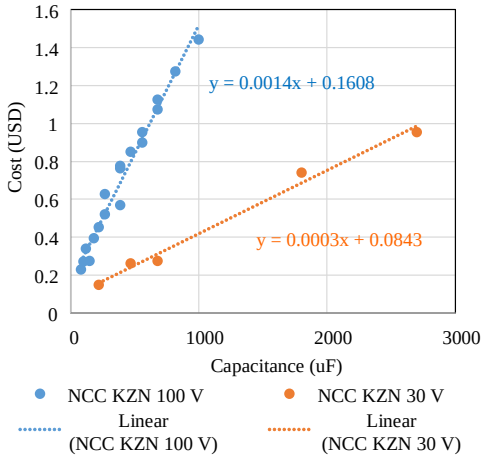

Fig. 19. Relation between capacitance and cost of electrolytic capacitor C_2.

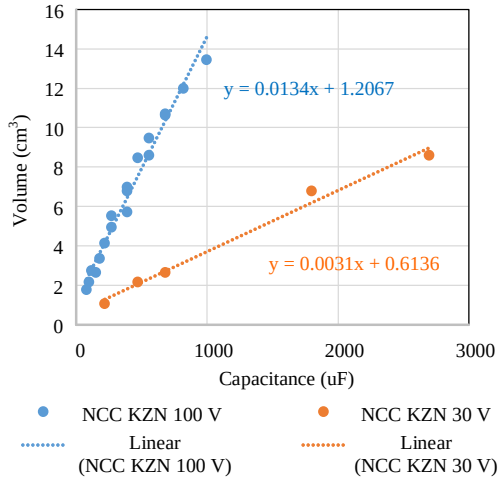

Fig. 18. Relation between capacitance and volume of electrolytic capacitor C_2.

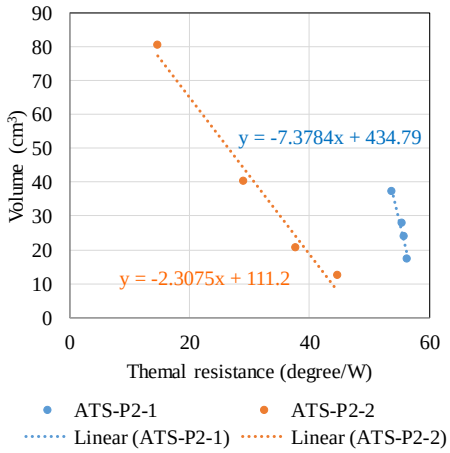

Fig. 20. Relation between thermal resistance and volume of heatsink.

$P_{\mathrm{sw_T}}$ is the switching loss. E_{on} and E_{off} are the turn on and turn off energy dissipated by the device, respectively.

The lifetime of the power switches is determined by the junction temperature. In this design, the estimated junction temperature should be limited to the maximum junction temperature to achieve certain lifetime target. Assuming the maximum temperature rise is $\Delta T_{\mathrm{j,max}}$, the maximum thermal resistance from junction to ambient can be obtained as

$$R_{\mathrm{ja}} = R_{\mathrm{jc}} + R_{\mathrm{ca}} \leq \frac{\Delta T_{\mathrm{j,max}}}{P_{\mathrm{ploss,sw}}} \tag{21}$$

where R_{jc} is the thermal resistance from junction to case, which can be obtained from the datasheet. R_{ca} is the thermal resistance from case to ambient (heat dissipation through the air or heat sink). Practically, the volume of the heatsink is linear with the thermal resistance. With larger volume and larger surface area to dissipate the heat, the thermal resistance is smaller, but cost will be higher. The volume and cost model for heat sink can be written in following equations and shown in Fig. 20 and Fig. 21, respectively.

$$Volume_{\mathrm{heatsink}} = k_{1,\mathrm{hs-vol}} R_{\mathrm{heatsink}} + k_{2,\mathrm{hs-vol}} \tag{22}$$

$$Cost_{\mathrm{heatsink}} = k_{1,\mathrm{hs-cost}} R_{\mathrm{heatsink}} + k_{2,\mathrm{hs-cost}} \tag{23}$$

where $k_{1,\mathrm{hs-vol}}$ and $k_{1,\mathrm{hs-cost}}$ represent the volume and cost coefficients related to thermal resistance, and $k_{2,\mathrm{hs-vol}}$ and $k_{2,\mathrm{hs-cost}}$ represent the package volume and cost, respectively. R_{heatsink} is the thermal resistance of the heat sink.

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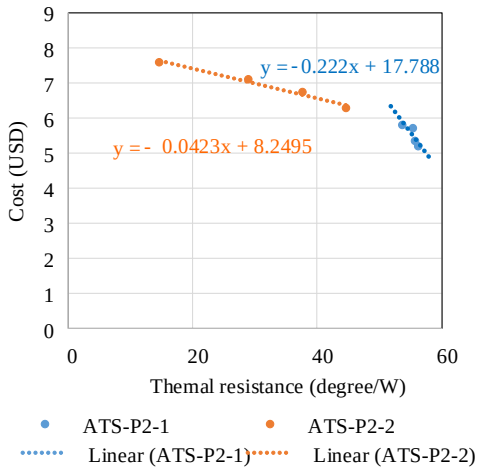


Fig. 21. Relation between thermal resistance and cost of heatsink.

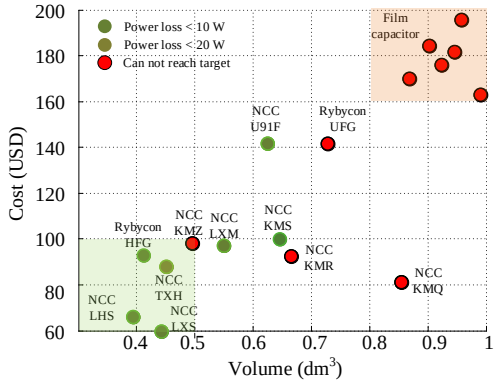


Fig. 22. Multi-objective optimization results based on different capacitor series.

(l) LC Filter Design

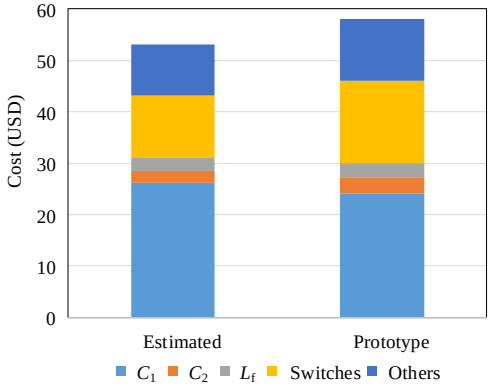
Inductor loss includes the core loss and winding loss, where the power loss model and data from Coilcraft are used [28]. The filter capacitor implemented is a small ceramic capacitor, whose loss, volume, and cost are not included. Compared with the electrolytic capacitor and power switches, the wear out failure rate of inductor and ceramic capacitor are much lower. Therefore, the lifetime estimation for the LC filter is ignored in this optimization.

(m) PCB, Analog and Digital ICs Design

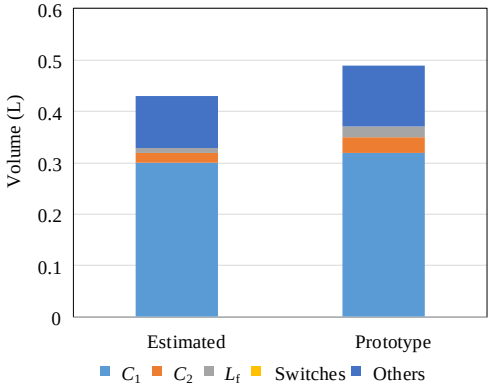
Beside the power stage, the auxiliary circuits and components for control and power supply also need to be taken into account for cost and volume. For simplicity, PCB losses (such as dielectric and conduction losses) are neglected. The losses of the auxiliary circuits include the gate driver loss and power consumption of the control electronics, which is assumed to be constant 3 W.

D. Design Results

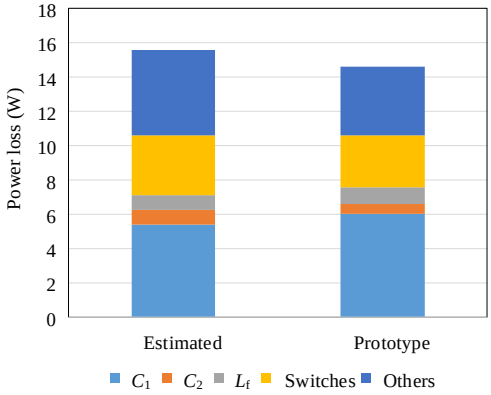
Following the design procedure discussed above, the performance space of all the possible choices can be obtained. The solution, which can achieve the lifetime target defined in Table. II will be selected. The lowest cost solutions with different capacitor manufacturers are shown in Fig. 22. It can be seen that the solutions with film capacitor has higher volume, cost, and power loss, compared with the active capacitor solution implemented with electrolytic capacitors using this design specification. The solution with Nippon Chemi-Con (NCC) LHS and NCC LXS electrolytic capacitor are the possible choices to achieve the lifetime target and all the design constraints in terms of cost, volume and power loss. The detail implementation of the NCC LXS solution will be discussed in Section IV.



(a) Cost comparison.



(b) Volume comparison.



(c) Power loss comparison.

Fig. 23. Comparison between the estimated performance and the prototype.

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TABLE IV
COMPONENT LIST OF THE PROTOTYPE.

Component	Part no.	Quantity	Unite price
Buffer capacitor C_1	Electrolytic capacitor 470 uF/ 450 V *6 ELXS451VSN471MA40S	6	4.3
Gate Driver for eGaN FETs	LM5113	2	2.8
GaN half-bridge	EPC2102/ 60 V/ 30 A	2	5.5
DC capacitor C_2	Electrolytic capacitor 2200 uF/ 35 V*3 EKZH350ELL222ML25S	3	0.7
Filter inductor	15 uH/ SER2918H-153KL	1	3.4
PWM isolator	SI8620EC-B-IS	2	1.6
Analog ICs	AD8615AUJZ-REEL7	4	1
Digital controller	DSPIC30F2020-30I/SO	1	4.4

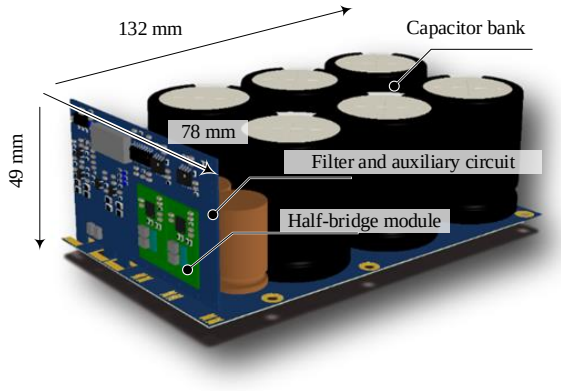

Fig. 24. Virtual prototype of the active capacitor for 5.5 kW single-phase inverter system.

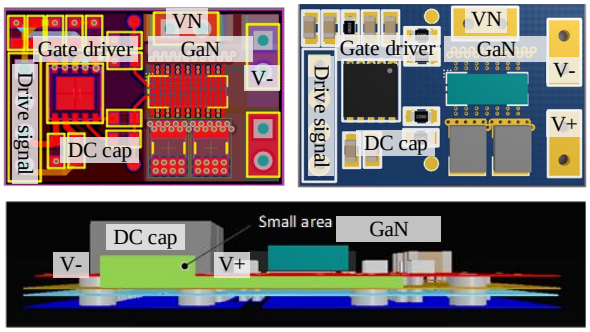

Fig. 25. Virtual prototype of the half-bridge power stage for the active capacitor.

IV. HARDWARE REALIZATION AND EXPERIMENTAL RESULTS

To verify the optimization results, an active capacitor prototype is build for 5.5 kW single-phase system. The component list is shown in Table. IV. C_1 is implemented by a 2800 μF capacitor bank, where NCC LXS 5000 hours/105 degree/ 470 uF/ 450 V high current capability electrolytic capacitor is used. Compared with the typical passive DC-link solution, 50 % capacitance reduction can be achieved. For the 5.5 kW single-phase system with DC-link voltage ranging from 320 V to 450 V, the maximum RMS current of the DC-link capacitor is $I_{\mathrm{RMS,C_1}} = \frac{P}{\sqrt{2}V_{\mathrm{DC-link}}}$=12.14 A. The maximum ripple voltage of C_1 as well as the DC voltage of C_2 is 9.77 V. The capacitor bank is implemented as 6*470 μF capacitors, whose thermal

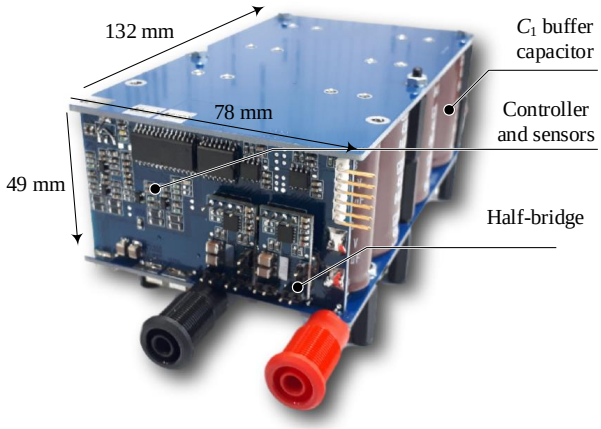

Fig. 26. Hardware prototype of the active capacitor for 5.5 kW single-phase inverter system.

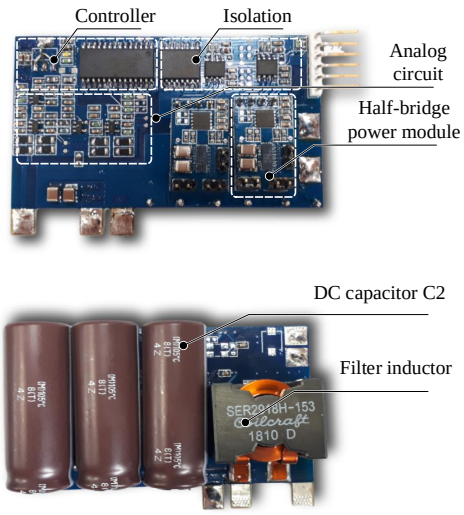

Fig. 27. Hardware prototype of the auxiliary circuit board of the active capacitor.

resistance from hot-spot to ambient is 14 K/W and from case to ambient is 10 K/W. Following the lifetime prediction method discussed in Section III, the lifetime can be estimated as 18 years (8 operating hours per day). Due to enough space around C_2 as shown in Fig.24, C_2 is implemented by a 6600

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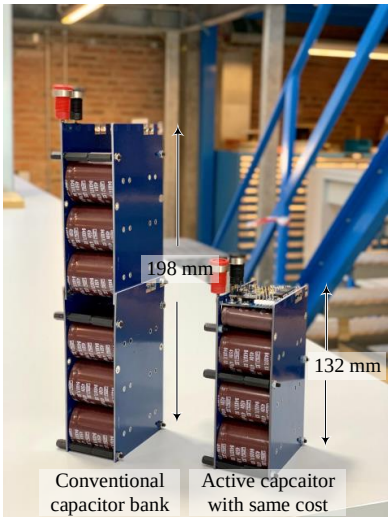

Fig. 28. Hardware prototype comparison between the passive capacitor bank and the active capacitor for 5.5 kW single-phase inverter system.

μF low-voltage capacitor bank (2200 μF*3) with the same dimension and higher height products from NCC KZH series. The capacitance is mainly limited by the current stress which is 5.5 A. Due to the modulation index is defined lower than 0.8, $V_{C_2,\mathrm{DC}}$ need to be higher than 12.2 V, which is selected as 15 V in this case. The power switches used in this design is 60 V GaN device from EPC 2102, where it can also be a MOSFET to reduce the cost. If the temperature rise limitation is 60 degree, a heatsink is not necessary. The benchmark between the estimated performance and the prototype are shown in Fig. 23. The physical performance of the prototype are compatible with the model based design in theory.

The virtual prototype is shown in Fig. 24. It contains of three parts: capacitor bank, half-bridge module and filter, and auxiliary circuit. Due to the capacitors are close to each other, the heat will transfer among them in the bank. In order to decouple the thermal coupling, the distance among the individual capacitors is 10 mm. The layout of the half-bridge module need to take special design. The gate drive loop and DC link loop is minimized for lower loop inductance as shown in Fig. 25. The current from DC positive to DC negative flows through the first and second layer of the PCB board, so the power loop is only the area between two PCB layers. In order to reduce the drive loop area, the drive IC is located next to the GaN device. The hardware prototype is shown in Fig. 26. The size is the same with the virtual prototype, where the volume is 0.5 L, which is on the same level with the optimization results and achieves the design constraints. The PCB board of the auxiliary circuit is shown in Fig. 27. On the top side of the PCB board, the circuit are separated into four area, in terms of controller, analog circuit for sampling, isolation for gate driver, and half-bridge power module. The bottom side is soldered with higher components, such as DC capacitors and filter inductor. Therefore, the space can be fully utilized. A comparison between the conventional passive capacitor bank and the designed active capacitor with the same cost are shown in Fig. 28, where 38 % volume reduction can be achieved by the active capacitor, compared with the conventional capacitor bank.

To verify the functionality and performance of the optimized active capacitor, the prototype is tested in the lab and connected to an equivalent single-phase system. The rated RMS current of the DC-link capacitor is 12 A, while the DC-link voltage ripple from peak to peak should be limited to 10 V. The testing condition ranges from 2 A to 12 A, and the electrical performance under different loading conditions are shown in Fig. 29. It can be seen that when the load current increases from 2 to 12 A, the DC-link voltage ripple raises from 1.8 V to 6 V, which can achieve the design target. The DC-link ripple of C_2 increases a little, but has no impact on the stability of the active capacitor, due to the large capacitance is implemented.

The thermal stresses of the power stage are shown in Fig. 30 in order to verify the reliability performance. During the testing, the ambient temperature in the lab is 30 degree. When the applied load changes from 2 A to 12 A, the maximum temperature will increase from 33 degrees to 94 degrees, which thereby is limited to 100 degrees. The maximum temperature rise is 64 degrees, which is at the same level as the calculations. The thermal stress of the buffer capacitor C_1 is shown in Fig. 31. The case temperature rises 7 degrees, which almost matches with the mathematical model, where the tested power loss is 0.6 W and the thermal resistance is 10 K/W.

In order to verify that the optimized solution can achieve better performance than other designs, the prototype with two different implementations is tested. As a case study, the performance under 100 kHz and 200 kHz switching frequency is benchmarked. Fig. 32 shows the power loss of these two cases. It can be seen that the 200 kHz case contribute to higher power loss. A comparison of the efficiency curve of the full-bridge auxiliary circuit with filters in two cases are shown in Fig. 33. The auxiliary circuit with 100 kHz switching frequency can achieve a higher efficiency. The temperature rise is also tested from the prototype, where the results are recorded in Fig. 34. The results are compatible with the trend of the power loss. From above benchmarking, it can be seen that the optimized prototype can achieve better performance by using 100 kHz switching frequency.

V. Conclusions

In this paper, a new design approach towards high performance active capacitor with lifetime, cost, volume, and power loss constraints is presented. The DC-link active capacitor is designed for a 5.5 kW single-phase system to limit the voltage ripple in full loading conditions. Different from the existing design with film and ceramic capacitors as the buffer capacitor, electrolytic capacitors are incorporated to minimize the life-cycle cost. Considering the electro-thermal modeling and lifetime estimation, the optimized solution can achieve the comparable lifetime, cost, and power loss with the conventional passive capacitor bank, but with a significant volume reduction. A prototype is realized in the lab to verify the multi-objective optimization. From the testing results, the following conclusions can be drawn:

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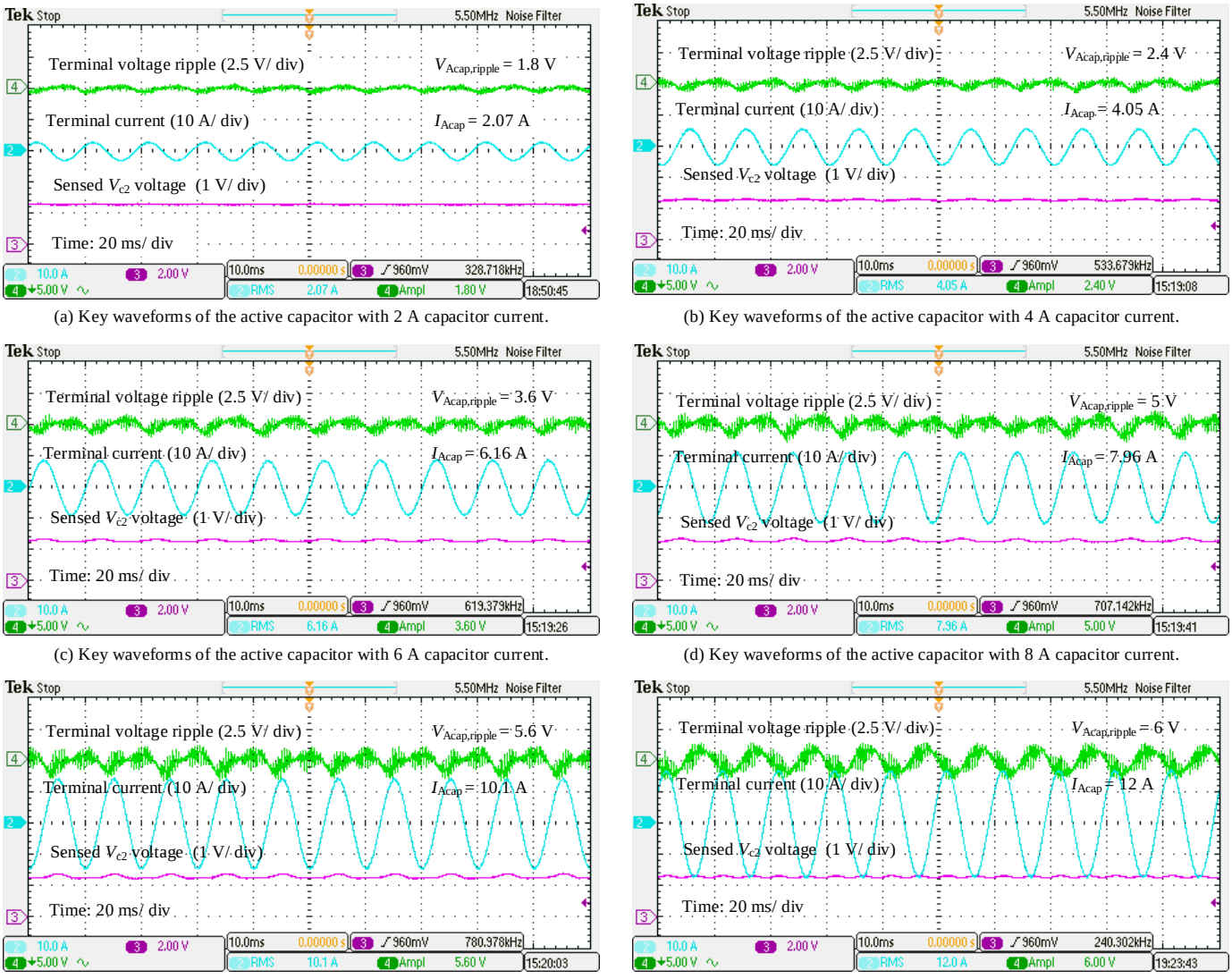

(a) Key waveforms of the active capacitor with 2 A capacitor current.

(b) Key waveforms of the active capacitor with 4 A capacitor current.

(c) Key waveforms of the active capacitor with 6 A capacitor current.

(d) Key waveforms of the active capacitor with 8 A capacitor current.

(e) Key waveforms of the active capacitor with 10 A capacitor current.

(f) Key waveforms of the active capacitor with 12 A capacitor current.

Fig. 29. Electrical waveforms of the active capacitor for 5.5 kW single-phase inverter system.

- With the proposed multi-objective optimization method, the lifetime of the active capacitor can be designed for 15 years by using electrolytic capacitors.
- The cost of the optimized design can be lower than 60 USD, which is the same level as the conventional passive capacitor bank solution.
- The volume of the active capacitor can be significantly reduced, which is only 62.5 % of the conventional solution.

ACKNOWLEDGEMENT

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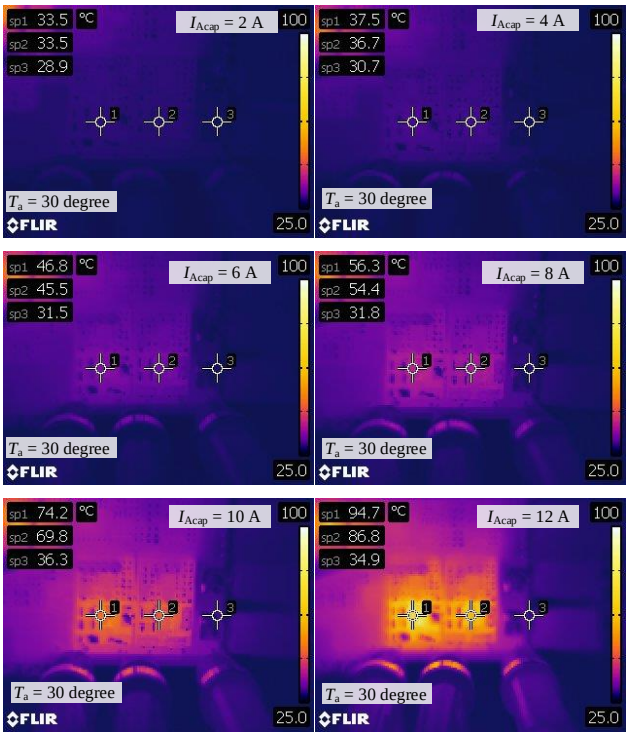

Fig. 30. Thermal stress of the half-bridge power switches.

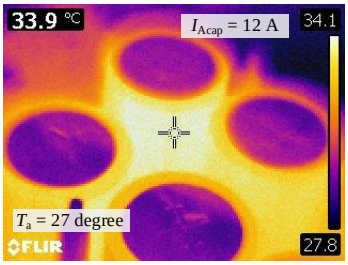

Fig. 31. Thermal stress of the buffer capacitor C_1.

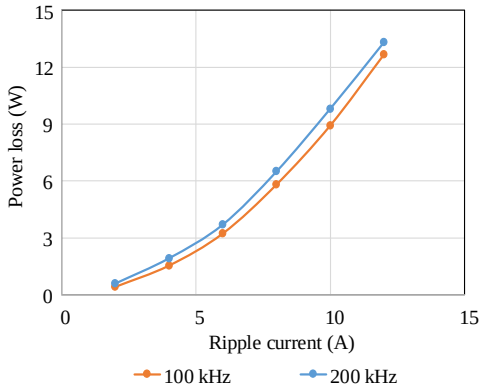

Fig. 32. Power loss of the active capacitor circuit with 100 kHz and 200 kHz switching frequency.

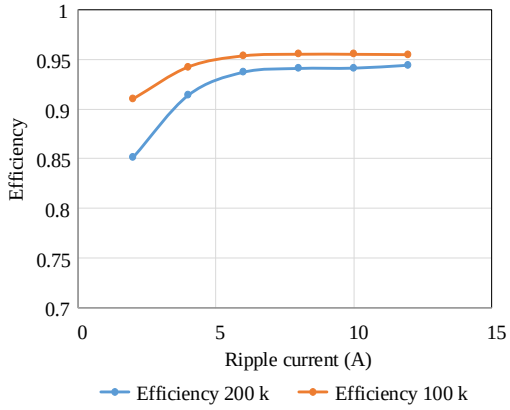

Fig. 33. Efficiency of the full-bridge auxiliary circuit of active capacitor with 100 and 200 kHz switching frequency.

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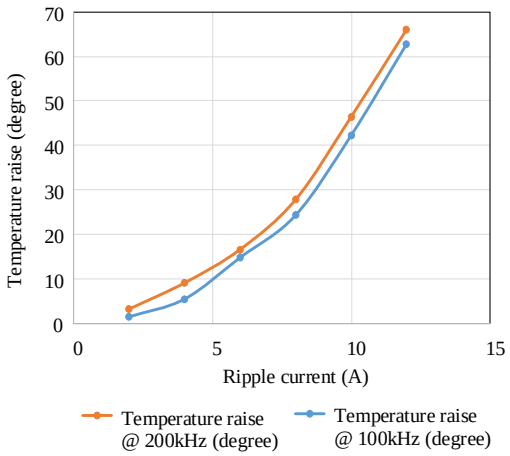
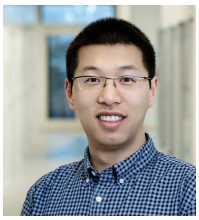


Fig. 34. Thermal stress of the half-bridge power switches of active capacitor with 100 and 200 kHz switching frequency at different loading conditions.



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